Application Note

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MPC500 Family Background Debug Mode

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The MPC500 family of microcontrollers offers a dedicated port to allow the debug of software. It is similar to the Background Debug Mode (BDM) interface on previous Motorola microcontroller families such as the MC68332, but is not electrically compatible. This application note explores some of the capabilities of the MPC500 family BDM interface software initialization requirements and part/revision identification. This application note also covers how to select which of the four possible MPC53*x*, MPC555, and MPC56*x* pin sets to use for the BDM port. The MPC53*x*, MPC555, and MPC56*x* BDM implementation differs slightly from the MPC509 BDM implementation and is the same as the MPC800 family BDM interface.

NOTE

The MPC509 is a discontinued product and is included only for historical comparison.

1 Entering BDM Mode on the MPC509, MPC555, MPC53*x*, and MPC56*x*

To enter BDM mode on power-up, the DSCK pin must be high. The DSCK pin is sampled on the rising edge of $\overline{\text{SRESET}}$. A high level will enable the Background Debug Mode. The DSDI pin is sampled 8 clocks after the rising edge of $\overline{\text{SRESET}}$ to set the clock mode of the BDM interface. If DSDI is low, the asynchronous (to the internal clock) mode is enabled which requires an external clock be used to clock data through the BDM interface. DSDI high (8 clocks after the rising edge of $\overline{\text{SRESET}}$) selects the synchronous mode of the BDM interface. The synchronous mode uses the internal system clock to transfer data into and out of the RCPU. Data must have proper setup and hold time to CLOCKOUT. Most debuggers use the asynchronous clock input to the DSCK pin.

BDM mode can be forced at reset on the MPC509, the MPC555, the MPC53*x*, and the MPC56*x* by connecting the DSCK pin through a 5.6K Ω resistor (6.1K Ω maximum) to 3.3 V (or 2.6 V for the MPC56*x*). This causes the device to enter debug mode immediately following reset. For production boards, the DSCK pin should be pulled down by a 10K Ω pull-down resistor (debuggers can drive this pin to force BDM mode). To disable BDM mode on a board that has been wired to enter BDM mode upon power-up, connect pin 4 (DSCK) of the BDM interface connector to pin 3 (Ground). To select the clock mode of the BDM interface on the MPC555 and the MPC56*x* devices, connect the DSDI pin through a 5.6K Ω (6.1K Ω is the maximum value) pull-down to VSS. (The weak 130 micro-amp driver must be overcome). The MPC509 can use a 10K Ω pull-down on DSDI.

2 BDM Port Signals

2.1 VFLS0/VFLS1 or FRZ

BDM connector pins 1 and 6

When both VFLS[0:1] pins are high, the RCPU processor is in a halted state. These pins also indicate the number of instructions that have been flushed from the history buffer due to an exception or miss-predicted branches for trace purposes under normal operation. In lieu of the VFLS[0:1] pins, the FRZ (freeze) pin can be used to indicate that the part is a halted debug state. In this case, the FRZ signal is connected to both pins 1 and 6 of the BDM connector.

NOTE

It is possible to determine whether the processor is halted in the debug state solely by looking at the Freeze status bit in the DSDO bitstream rather than using the VFLS[0:1] or FRZ pins. Most debuggers do not support this configuration.

2.2 $\overline{\text{RESETOUT}}$ (MPC509) / $\overline{\text{SRESET}}$ (MPC555/MPC53*x*/MPC56*x*)

BDM connector pin 2

On the MPC509, $\overline{\text{RESETOUT}}$ is an output only. On the MPC555, MPC53*x*, and MPC56*x* devices, $\overline{\text{SRESET}}$ is bidirectional and can be driven by the debugger. Usually, it is used as a reset out of the processor. Debug software should monitor the $\overline{\text{RESETOUT}}$ or $\overline{\text{SRESET}}$ pins to determine if the RCPU is in a reset state.

2.3 DSCK

BDM connector pin 4

DSCK is the input clock to the debug port when used in asynchronous mode. The synchronous mode (enabled by DSDI being high 8 clocks after $\overline{\text{SRESET}}$) uses the internal system clock. When using the internal system clock, the DSDI input signal must respect the setup and hold times of the internal system clock. It does allow debug messages to be input and output at the same frequency as the system clock. When using the asynchronous mode, DSCK should have a maximum frequency of one-third of the system clock.

2.4 $\overline{\text{RESET}}$ (MPC509) / $\overline{\text{HRESET}}$ (MPC555/ MPC53*x*/MPC56*x*)

BDM connector pin 7

$\overline{\text{RESET}}$ on the MPC509 is an input only. $\overline{\text{HRESET}}$ on the MPC555, MPC53*x*, and MPC56*x* devices is bidirectional, but is primarily used as the hard reset into the RCPU core processor. $\overline{\text{RESET}}$/$\overline{\text{HRESET}}$ allows the debugger to reset the RCPU processor.

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2.5 DSDI

BDM connector pin 8

The DSDI (debug serial data input) allows instructions and data to be clocked into the RCPU processor. The DSDI input message consists of a start bit (high) followed by a mode bit, a control bit, and either a 7-bit trap enable instruction or a normal 32-bit normal instruction. The debugger should wait for the “ready” signal on the DSDO output before beginning an input message. See the Development Support section of the MPC555, MPC53*x*, or MPC56*x* Reference Manuals for more information.

2.6 DSDO

BDM connector pin 10

The DSDO (debug serial data output) allows information to be clocked out of the RCPU processor. The DSDO output indicates that the development port is “ready” for a new input message by negating its output (driving it low). The DSDO output message is clocked out synchronous to the DSDI input message. The message consists of a ready bit (low) followed by two status bits and either a 7-bit trap enable message or a 32-bit data message. See the Development Support section of the MPC555, MPC53*x* or MPC56*x* Reference Manuals for more information.

NOTE

Depending on the operation requested, it may take several input messages (NOP commands can be shifted in) for the desired results to be available from the development port.

2.7 Ground

BDM connector pins 3 and 5

The Ground pins provide a ground reference for the BDM port.

2.8 Power

BDM connector pin 9

The power pin of the BDM connector should be connected to the core processor’s main power supply. On the MPC509 and the MPC555, the power supply should be 3.3 V. On the MPC53*x* and MPC56*x* parts, it should be 2.6 V. This configuration, which allows debug hardware to monitor whether power is applied to the microcontroller, can be used as a reference for determining the BDM interface voltage (for setting the input voltage of the BDM interface).

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3 MPC509 BDM Port

Table 1. MPC509 BDM Port

VFLS0 (pin 69)	1	• •	2	$\overline{\text{RESETOUT}}$ (pin 38)
GROUND	3	• •	4	DSCK (pin 44)
GROUND	5	• •	6	VFLS1 (pin 68)
$\overline{\text{RESET}}$ (pin 39)	7	• •	8	DSDI (pin 45)
Power (+3.3 V)	9	• •	10	PLL/DSDO (pin 73)

No software initialization is required to use the MPC509 BDM interface once it is enabled at power-up.

4 MPC555/MPC556, MPC53*x*, and MPC56*x* Hardware BDM Options

Due to various application requirements, there are 3 possible MPC555, MPC53*x*, and MPC56*x* BDM connector pinouts. In addition, there is a fourth option available does not use the VFLS[0:1] or FRZ signals and determines the freeze status solely on information clocked out of the MPC55*x* and MPC56*x* debug port. However, this option is not supported on all debuggers. While the BDM pin option can be chosen based on the application, there are preferred pinouts for specific applications. Table 2 shows the options for the VFLS0 and VFLS1 or FRZ signals on the BDM connector. Motorola recommends that Option A be used on development systems that require maximum debug capability. Option B is the default power-on reset condition. Some Motorola evaluation boards support both modes A and B, but some support only mode B.

Table 2. MPC555 VFLS BDM Pin Options

Option	Signals Used on the BDM Connector	MPC555 Package Ball	MPC565/ MPC535 Package Ball	MPC561/ MPC563/ MPC533 Package Ball	Program Trace Capable	System Limitations
A	VFLS0/MPIO32B3 VFLS1/MPIO32B4	J18 K18	M26 N24	M25 M26	Yes	2 GPIO pins lost.
B	IWP0/VFLS0 IWP1/VFLS1	L2 L1	T3 R4	N2 N3	Yes	2 Instruction Watchpoint pins lost.
C	SGPIO6/FRZ/$\overline{\text{PTR}}$	K3	T4	N4	No	1 GPIO pin lost.
D	—	—	—	—	Yes	Debugger BDM software driver must support sampling the Freeze status bit in the DSDO bitstream.

WARNING

For the MPC555, the voltage levels of the BDM output signals are 0 to 3.3 V. The MPC53*x* and MPC56*x* devices have 2.6-V outputs. Not all BDM tools can interface to the lower voltage outputs. Customers should insure that their tool is compatible to the device or install level shifters on the BDM output signals (DSDO and VFLS[0:1]). It is permissible to drive the inputs with 5 V signals on all of the parts.

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4.1 Option A: Maximum Debug Capability

Table 3. MPC555/MPC556 BDM Option A

VFLS0/MPIO32B3 (ball J18)	1	•	2	$\overline{\text{SRESET}}$ (ball V20)
GROUND	3	•	4	TCK/DSCK (ball J1)
GROUND	5	•	6	VFLS1/MPGIO32B4 (ball K18)
$\overline{\text{HRESET}}$ (ball W20)	7	•	8	TDI/DSDI (ball K2)
Power (+3.3 V)	9	•	10	TDO/DSDO (ball J2)

Table 4. MPC565/MPC566 and MPC535/MPC536 BDM Option A

VFLS0/MPIO32B3 (ball M26)	1	•	2	$\overline{\text{SRESET}}$ (ball AC24)
GROUND	3	•	4	TCK/DSCK (ball L2)
GROUND	5	•	6	VFLS1/MPGIO32B4 (ball N24)
$\overline{\text{HRESET}}$ (ball AB23)	7	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	10	TDO/DSDO (ball R2)

Table 5. MPC561/MPC562, MPC563/MPC564, and MPC533/MPC534 BDM Option A

VFLS0/MPIO32B3 (ball M25)	1	•	2	$\overline{\text{SRESET}}$ (ball W24)
GROUND	3	•	4	TCK/DSCK (ball L2)
GROUND	5	•	6	VFLS1/MPGIO32B4 (ball M26)
$\overline{\text{HRESET}}$ (ball W23)	7	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	10	TDO/DSDO (ball M4)

Option A allows for the maximum debug capability for BDM and program trace signals. This mode uses two GPIO pins and can have zero, two, or four instruction watchpoints. To use the Agilent Technologies (Hewlett Packard) Prototype Analyzer for program trace, this option should be used.

Table 6. Option A Configuration Options

SIUMCR [DBGC]	Program Trace Capable (VF[0:2] Available)	Bus Arbitration Signals Available ($\overline{\text{BG}}$, $\overline{\text{BR}}$, & $\overline{\text{BB}}$)	Instruction Watchpoints Available (IWP[0:3])	Data Watchpoints Available (LWP[0:1])	GPIO Pins Used
00	Yes	Yes	0	Up to 1	2 [1]
01	Yes	Yes	2	Up to 1	2
10 [2]	Yes	No	0	Up to 1	2
11	Yes	No	4	Up to 2	2

1 5 GPIO pins are lost if both the VF and VFLS signals are enabled. Some versions of the MPC555 have an errata that requires both VF and VFLS be enabled or disabled together.

2 This selection duplicates the VF[0:2] and VFLS[0:1] on both the $\overline{\text{VFLS}}$[0:1]/MPIO32B[3:4] and $\overline{\text{IWP}}$[0:1]/VFLS[0:1] pins and on the VF[0:2]/MPIO32B[0:2], and $\overline{\text{BG}}$/VF[0]/LWP[1], $\overline{\text{BR}}$/VF[1]/IWP[2], $\overline{\text{BB}}$/VF[2]/IWP[3].

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4.1.1 Software Initialization Requirements

The VFLS0_MPIO32B3 and VFLS1_MPGIO32B4 pins power-up as general purpose outputs that are driven weakly high (5 V) during reset. To change these pins to the VFLS0/VFLS1, the VFLS bit (0x01) must be set in the MIOS1TPCR (0x0030 6800). Due to errata number AR_128, which applies to the early revisions of the MPC555 silicon, the VFLS and the VF MIOS pin configurations must be set the same (that is, the MIOS1TPCR should be set to 0x3). This is fixed for MPC555 mask sets K62N or later.

NOTE

On reset these two pins will be driven weakly to 5 V. After they are programmed to the VFLS function, they will be 0 to 3.3 V.

When used with an Agilent Emulation probe (Run Control), the VFLS[0:1] pins may each need a 10K Ω pull-up resistor to 3.3 V (MPC555/MPC556) or 2.6 V (MPC53*x* and MPC56*x*). (The internal weak pull-up resistor may not be sufficient to overcome the input current requirements of the Agilent Probe TIMs board.)

NOTE

On future MPC5xx family devices (MPC565), these pins could have weak pull-down resistors. In addition, on future devices, all BDM signals have logic levels of 0 and 2.6 V. For the MPC53*x* and MPC56*x*, external pull-up resistors are required and should be 3.8K Ω or less at any time the VFLS0_MPIO32B3 and VFLS1_MPGIO32B4 are used for the BDM interface.

4.2 Option B: Maximum External Bus Capability

Table 7. MPC555/MPC556 BDM Option B

IWP0/VFLS0 (ball L2)	1	•	•	2	$\overline{\text{SRESET}}$ (ball V20)
GROUND	3	•	•	4	TCK/DSCK (ball J1)
GROUND	5	•	•	6	IWP1/VFLS1 (ball L1)
$\overline{\text{HRESET}}$ (ball W20)	7	•	•	8	TDI/DSDI (ball K2)
Power (+3.3 V)	9	•	•	10	TDO/DSDO (ball J2)

Table 8. MPC535/MPC536 and MPC565/MPC566 BDM Option B

IWP0/VFLS0 (ball T3)	1	•	•	2	$\overline{\text{SRESET}}$ (ball AC24)
GROUND	3	•	•	4	TCK/DSCK (ball L2)
GROUND	5	•	•	6	IWP1/VFLS1 (ball R4)
$\overline{\text{HRESET}}$ (ball AB23)	7	•	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	•	10	TDO/DSDO (ball R2)

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Table 9. MPC533/MPC534, MPC561/MPC562, and MPC563/MPC564 BDM Option B

IWP0/VFLS0 (ball N2)	1	•	•	2	$\overline{\text{SRESET}}$ (ball W24)
GROUND	3	•	•	4	TCK/DSCK (ball L2)
GROUND	5	•	•	6	IWP1/VFLS1 (ball N3)
$\overline{\text{HRESET}}$ (ball W23)	7	•	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	•	10	TDO/DSDO (ball M4)

Option B is defined to allow the maximum external debug capability. It should be used in complex systems that require additional bus control, such as those that use multiple processors on the same bus.

Table 10. Option B Configuration Options

SIUMCR [DBGC]	Program Trace Capable (VF[0:2] Available)	Bus Arbitration Signals Available (BG, BR, & BB)	Instruction WatchPoints Available (IWP[0:3])	Data WatchPoints Available (LWP[0:1])	GPIO Pins Used
00	No	Yes	0	Up to 1	0
10	Yes	No	0	Up to 1	0

4.2.1 Software Initialization Requirements

The IWP0/VFLS0 and IWP1/VFLS1 pins power-up functioning as VFLS0 and VFLS1. To keep these pins as the VFLS[0:1] function, the DBGC bits [9:10] in the SIUMCR (0x002F C000) must be set to 0b00 (default after $\overline{\text{PORESET}}$ negation) or to 0b10. The setting of the DBGC depends on the functions required for other pins controlled by the DGBC bits ($\overline{\text{BI}}$/STS, $\overline{\text{BG}}$/VF0/LWP1, $\overline{\text{BR}}$/VF1/IWP2, and $\overline{\text{BB}}$/VF2/IWP3). They can also be programmed via either the internal or external reset configuration word (data bus bits 9 and 10).

4.3 Option C: Maximum I/O Configuration

Table 11. MPC555/MP556 BDM Option C

SGPIO6/FRZ/$\overline{\text{PTR}}$ (ball K3)	1	•	•	2	$\overline{\text{SRESET}}$ (ball V20)
GROUND	3	•	•	4	TCK/DSCK (ball J1)
GROUND	5	•	•	6	SGPIO6/FRZ/$\overline{\text{PTR}}$ (ball K3)
$\overline{\text{HRESET}}$ (ball W20)	7	•	•	8	TDI/DSDI (ball K2)
Power (+3.3 V)	9	•	•	10	TDO/DSDO (ball J2)

Table 12. MPC535/MPC536 and MPC565/MPC566 BDM Option C

SGPIO6/FRZ/$\overline{\text{PTR}}$ (ball T4)	1	•	•	2	$\overline{\text{SRESET}}$ (ball AC24)
GROUND	3	•	•	4	TCK/DSCK (ball L2)
GROUND	5	•	•	6	SGPIO6/FRZ/$\overline{\text{PTR}}$ (ball T4)
$\overline{\text{HRESET}}$ (ball AB23)	7	•	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	•	10	TDO/DSDO (ball R2)

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Table 13. MPC533/MPC534, MPC561/MPC562, and MPC563/MPC564 BDM Option C

SGPIO6/FRZ/$\overline{\text{PTR}}$ (ball N4)	1	•	•	2	$\overline{\text{SRESET}}$ (ball W24)
GROUND	3	•	•	4	TCK/DSCK (ball L2)
GROUND	5	•	•	6	SGPIO6/FRZ/$\overline{\text{PTR}}$ (ball N4)
$\overline{\text{HRESET}}$ (ball W23)	7	•	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	•	10	TDO/DSDO (ball M4)

Option C allows the maximum use of IO capability. The FRZ signal is used to indicate that the processor is stopped.

Table 14. Option C Configuration Options

SIUMCR [DBGC]	Program Trace Capable (VF[0:2] Available)	Bus Arbitration Signals Available (BG, BR, & BB)	Instruction WatchPoints Available (IWP[0:3])	Data WatchPoints Available (LWP[0:1])	GPIO Pins Used (FRZ/PTR/SGPIO6)
00	Yes	Yes	0	up to 1	2
10	Yes	No	0	up to 1	2

4.3.1 Software Initialization Requirements

The SGPIO6/FRZ/$\overline{\text{PTR}}$ pin powers-up as a Program Trace function ($\overline{\text{PTR}}$). By default, on the MPC555, $\overline{\text{PTR}}$ will be high after reset. On the MPC53*x* and MPC56*x*, however, $\overline{\text{PTR}}$ will be pulled low and requires an external pull up resistor (3.8 kΩ or less) to 2.6 V. To change this pin to the Freeze function, the GPC bits [13:14] in the SIUMCR (0x002F C000) must be set to 0b10 or 0b11.

4.4 Option D: Software Freeze Detection

Table 15. MPC555/MPC556 BDM Option D

N/C	1	•	•	2	$\overline{\text{SRESET}}$ (ball V20)
GROUND	3	•	•	4	TCK/DSCK (ball J1)
GROUND	5	•	•	6	N/C
$\overline{\text{HRESET}}$ (ball W20)	7	•	•	8	TDI/DSDI (ball K2)
Power (+3.3 V)	9	•	•	10	TDO/DSDO (ball J2)

Table 16. MPC535/MPC536 and MPC565/MPC566 BDM Option D

N/C	1	•	•	2	$\overline{\text{SRESET}}$ (ball AC24)
GROUND	3	•	•	4	TCK/DSCK (ball L2)
GROUND	5	•	•	6	N/C
$\overline{\text{HRESET}}$ (ball AB23)	7	•	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	•	10	TDO/DSDO (ball R2)

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Table 17. MPC533/MPC534, MPC561/MPC562, and MPC563/MPC564 BDM Option D

N/C	1	•	•	2	$\overline{\text{SRESET}}$ (ball W24)
GROUND	3	•	•	4	TCK/DSCK (ball L2)
GROUND	5	•	•	6	N/C
$\overline{\text{HRESET}}$ (ball W23)	7	•	•	8	TDI/DSDI (ball M1)
Power (+2.6 V)	9	•	•	10	TDO/DSDO (ball M4)

Option D requires that the DSDO messages be monitored to detect that the processor is stopped.

4.4.1 Software Initialization Requirements

Software initialization of the part is not required to use the Freeze status bit in the DSDO message. It does require that the debugger input a NOP trap mode command (0b111000000) into the DSDI pin and monitor the DSDO message out of the device to determine if the part is halted in debug mode or if it is still executing instructions by checking the Freeze status bit in the DSDO message. See Table 18 for the DSDO message format.

NOTE

Do not use this option unless it has been confirmed that the tool (debugger) to be used supports this option. Most debuggers available do not support this option.

Table 18. Status / Data Shifted Out of Development Port Shift Register

Ready	Status [0:1]		Data			Function
			Bit 0	Bit 1	Bits [2:31] or [2:6] (Depending on Input Mode)	
(0)	0	0	Data			Valid Data from CPU
(0)	0	1	Freeze status [1]	Download in progress [2]	1's	Sequencing Error
(0)	1	0			1's	CPU Interrupt
(0)	1	1			1's	Null

[1]The Freeze status bit is set to 1 when the CPU is in debug mode and is cleared to 0 otherwise.

[2]The Download in Progress status bit is asserted (0) when Debug port in the Download procedure and is negated (1) otherwise.

5 Differences Between the MPC509, MPC800, and MPC555/MPC53*x*/MPC56*x* BDM Ports

The MPC555, MPC53*x*, and MPC56*x* BDM ports are based on the MPC800 BDM port, not the MPC509. The MPC800 BDM port was an enhancement of the MPC509 BDM port. The following list describes the primary differences between the MPC509 BDM to the MPC800 BDM:

- The MPC800 includes a Freeze status bit in the DSDO bitstream. The Freeze status bit is output as bit 0 of the data stream when the status[0:1] bits equal 0b01, 0b10, or 0b11. The Freeze bit is high (1) when the MCU is in debug mode and is low (0) otherwise.

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- The MPC800 supports a fast download mode to allow memory to be loaded more quickly than the first generation (MPC509) BDM design. The Download In Progress is output on bit 1 of the DSDO data stream when the status[0:1] bits equal 0b01, 0b10, or 0b11. The Download In Progress bit is high (1) when in the Download procedure and is low (0) otherwise.

More information on the BDM bitstream is available in Section 21 (Development Support) of the MPC555 User's Manual and Section 8 of the MPC509 Reference Manual.

NOTE

All of the MPC500 and MPC800 devices require that an **isync** instruction be executed upon entering BDM mode when the core processor is running in non-serialized mode.

6 Identifying the Correct Processor and Version

6.1 The Processor Version Register (PVR)

The processor version register (PVR) is a special processor register, and is read with an **mtspr** instruction. The PVR (SPR287) defines the type of core that is present in the microcontroller. Bits [0:15] hold the version of the CPU core and bits [16:31] hold the revision number of that core. Table 19 shows the currently defined PVR version values.

Table 19. PVR Values

Core Version	RCPU Core Type	Currently Defined Parts
0002	RISC PPC core with floating point	MPC509, MPC533/MPC534, MPC535/MPC536, MPC555/MPC556, MPC561/MPC562, MPC563/MPC564, and MPC565/MPC566
0050	Fixed point RISC PPC core	MPC821, MPC823, MPC860

The PVR revision number of the MPC509, MPC533, MPC534, MPC535, MPC536, MPC555, MPC561, MPC563, and MPC565 is 0x0020.

Since the MPC555, MPC53*x*, and MPC56*x* PVR is the same as the MPC509, the IMMR (SPR638) must be read to determine the actual part number. The MPC509 does not have a IMMR and will get an error when accessed.

6.2 The Internal Memory Map Register (IMMR)

The IMMR (SPR638) bit definition for the MPC53*x*, MPC555, and MPC56*x* is different than the MPC800-family IMMR bit definition. For the MPC800 family, the PARTNUM and MASKNUM are in the lower portion of the register (bits [16:31]). For the MPC53*x*, MPC555 and MPC56*x* devices, these fields are located in the upper portion of the register (bits [0:15]).

- The PARTNUM is bits [0:7] and the MASKNUM is in bits [8:15] on the MPC53*x*, MPC555, and MPC56*x*.
- The PARTNUM is bits [16:23] and the MASKNUM is in bits [24:31] for the MPC800 family.

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Table 20. Currently Defined Part Numbers

PARTNUM	Device
0x00	MPC860/MPC821
0x10	MPC801
0x20	MPC823
0x30	MPC555/MPC556
0x33	MPC565/MPC566 or MPC535/MPC536
0x34	MGT560
0x35	MPC561/MPC562
0x36	MPC563/MPC564 or MPC533/MPC534

NOTE

The J12F mask set of the MPC555 has an incorrect part number (0x04). This was fixed in the next revision (J76N) and later mask sets.

Table 21. MPC555 Mask Sets

Mask Set	Nickname	PARTNUM	MASKNUM	Part Number Marking [1]
J12F	A,C	0x04	0x00	—
3J76N	G	0x30	0x10	—
0K02A/1K02A/ 2K02A	K	0x30	0x20	—
5K02A/0K83H/ 2K83H	K2	0x30	0x31	MPC555LF4MZP40 [2]
6K02A/1K83H/ 3K83H/5K83H	K3	0x30	0x32	MPC555LFMZP40 [2]
K62N/1K62N/ 1K06S	M	0x30	0x40	MPC555LF8MZP40 [2]

1 On devices that do not have the mask set marked on the device, the part number differentiates between revisions.
2 Commercial temperature range (–40 to +85 C) devices are marked with a C instead of an M. For example, MPC555LFCZP40 instead of MPC555LFMZP40.

Table 22. MP561/MPC562 Mask Sets

Mask Set	Nickname	PARTNUM	MASKNUM	Part Number Marking [1]
0K27S	0	0x35	0x00	—
0L40B	A	0x35	0x10	—
0L17K	C	0x35	0x20	MPC561MZP56 [2, 3, 4]
L05S	D	0x35	0x30	MPC561MZP56 REV D [2, 3, 4]

1 On devices that do not have the mask set marked on the device, the part number differentiates between revisions.
2 Commercial temperature range (–40 to +85 C) devices are marked with a C instead of an M. For example, MPC561CZP56 instead of MPC561MZP56.
3 The speed field could be 40 instead of 56 for a 40 MHz versus a 56MHz part.
4 The part number field will be 562 (instead of 561) for parts that support code compression.

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Table 23. MPC563/MPC564 Mask Sets

Mask Set	Nickname	PARTNUM	MASKNUM	Part Number Marking [1]
0K73X/1K73X	0,0a	0x36	0x00	—
0L74H	A	0x36	0x10	MPC563MZP56[4]
0L08N	B	0x36	0x20	MPC563MZP56 REV B [2, 3, 4]

1 On devices that do not have the mask set marked on the device, the part number differentiates between revisions.
2 Commercial temperature range (–40 to +85 C) devices are marked with a C instead of an M. For example, MPC563CZP56 instead of MPC563MZP56.
3 The speed field could be 40 instead of 56 for a 40 MHz versus a 56 MHz part.
4 The part number field will be 564 (instead of 563) for parts that support code compression.

Table 24. MP565 Mask Sets

Mask Set	Nickname	Part Num	Mask Num	Part Number Marking [1]
1K85H	0a	0x33	0x00	—
K16Y	A	0x33	0x10	—
1K16Y	B	0x33	0x11	—
2K16Y	C	0x33	0x11	MPC565MZP56 [2, 3, 4]
L99N	D	0x33	0x20	MPC565MZP56 REV D [2, 4, 4]

1 On devices that do not have the mask set marked on the device, the part number differentiates between revisions.
2 Commercial temperature range (–40 to +85 C) devices are marked with a C instead of an M. For example, MPC565CZP56 instead of MPC565MZP56.
3 The speed field could be 40 instead of 56 for a 40 MHz versus a 56 MHz part.
4 The part number field will be 566 (instead of 565) for parts that support code compression.

7 MPC500 BDM Versus JTAG on Power-up

Since the BDM pins on all MPC500 devices are shared between the BDM and JTAG functions, the initial function must be defined at power-up. Different members of the MPC500 family have different methods of selecting between the BDM and JTAG functions.

NOTE

JTAG is implemented for Boundary Scan operations only. JTAG does not have provide access to the internal circuitry of the device.

7.1 MPC555 BDM Versus JTAG Selection

On the MPC555, the state of the shared BDM/JTAG pins is based on the DBPC bit of the SIUMCR. The default is read from the internal data bus bit 11 (DBPC) of the reset configuration word. The default external reset configuration word ($\overline{\text{RSTCONF}}$ = 1) is all low (0x0000 0000); that is, it powers up with BDM pins enabled. If an external reset configuration word is used, data bus pin 11 needs to be low during reset. To enable JTAG mode, data bus bit 11 (DBPC) and data bus bit 16 (PRPM peripheral mode enable) must be

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held high during reset. If the internal Flash reset config word is selected ($\overline{\text{RSTCONF}}$ = 1 and $\overline{\text{HC}}$ = 0, [$\overline{\text{HC}}$ is bit 20 of the Flash reset config word]), then bit 11 of the Flash reset config word needs to be cleared (0).

WARNING

If the internal Flash reset config word is selected ($\overline{\text{RSTCONF}}$ = 1 and $\overline{\text{HC}}$ = 0) and bit 11 of the Flash RCW is set (1), then the BDM pins are disabled (the JTAG functions are enabled) and the user will not be able to program the Flash or access the device via BDM mode.

7.2 MPC535/MPC536 and MPC565/MPC566 BDM Versus JTAG Selection

The mode of the shared BDM/JTAG pins is selected based on the state of the JCOMP pin. A 0 on JCOMP enables the BDM pin functions. If JCOMP = 1 then JTAG mode is enabled and the JTAG functions will be selected.

7.3 MPC561/MPC562, MPC563/MPC564, and MPC533/MPC534 BDM Versus JTAG Selection

The mode of the shared BDM/JTAG pins is selected at $\overline{\text{PORESET}}$ negation based on the state of the JCOMP pin. A 0 on JCOMP enables the BDM or Nexus pin functions. If JCOMP = 1 then JTAG mode is enabled and the JTAG functions will be selected. These pins can be used as Nexus pins if the JCOMP/$\overline{\text{RSTI}}$ pin is negated prior to the negation of $\overline{\text{HRESET}}$ (but after $\overline{\text{PORESET}}$ is negated).

8 Other MPC555, MPC53*x*, and MPC56*x* Initialization

The software watchdog is enabled on reset in BDM mode on the MPC555. To disable the software watchdog, write a value of 0x0000FF00 to the SYPCR (0x2FC004). Note that this is a write-once register after a power-on reset. In addition, the bus monitor is enabled in BDM mode and may need to be initialized. When in BDM mode the ICTRL and DER registers can only be changed from the debug port. Writes to the development support registers from within executing software will be ignored. The below listing shows the minimal initialization via the BDM port. This code should be transferred into the device via the 37-bit DSDI messages and should follow the downloading of code to memory. This example uses a start (execution) address of 0x3F9800 (the start of the MPC555 internal SRAM).

- Turn off software watchdog (if needed)
  - Set 0x2FC004 = 0x0000FF80
- Change clock frequency (if needed)
  - Set 0x2FC284 = 0x00400000 (for 40 MHz with 4 MHz in)
  - Set 0x2FC284 = 0x00100000 (for 40 MHz with 20 MHz in)
- Download code to the target microcontroller
- Set DER to allow all exceptions to return to BDM mode
  - Set SPR_149 (DER) = 0x7FE7540F

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- Read current value of the MSR to determine IP (instruction pointer) setting
- Set SRR1 to desired MSR register (Floating Point enable, Machine Check enable, Recoverable Interrupt Enable - other options if needed, set IP as read in previous step).
  - Write SRR1 = 0x000003002
- Set the program counter by setting SRR0
  - Write SRR0 = execution address
- Read the ECR register to clear out any exceptions
  - Read SPR_148 (ECR)
- Set up the stack by setting the PPC General Purpose register 1 to a valid SRAM location
  - Set R1 = some free area of internal SRAM (for example 0x3FFFF0)
- Enter run mode by inputting an RFI instruction to begin execution. This loads the MSR and IP to the values from SRR0 and SRR1.
  - RFI

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